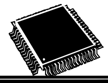
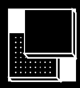
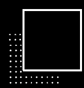
[redacted]ARM7TDMI™ 32-BIT MCU WITH FLASH[redacted]
[redacted]TIMERS, ADC, 10 COMMUNICATIONS IN[redacted]

- ■ [redacted]ore
  - – ARM7TDMI 32-bit RISC CPU
  - – 59 MIPS @ 66 MHz from SRAM
  - – 45 MIPS @ 50 MHz from Flash
- ■ **Memories**
  - – Up to 256Kbytes Flash program memory (10 kcycles endurance, 20 yrs retention)
  - – 16K bytes Flash data memory (100 kcycles endurance, 20 yrs[redacted]
  - – [redacted]p to 64 Kbytes RA[redacted]
  - – [redacted]ernal M[redacted] banks[redacted]
  - – Multi-bo[redacted]
- ■ **Clock, Res**[redacted]
  - – 3.0 to 3.6V [redacted] face
  - – Internal 1.8V vo[redacted]
  - – Clock input from 0[redacted]
  - – Embedded RTC oscillator running from external 32 kHz crysta[redacted]
  - – Embedded PLL for CPU[redacted]
  - – Realtime Clock for clock-c[redacted]
  - – 5 power saving modes: SLO[redacted] LPWAIT, STOP and STANDB[redacted]
- ■ **Nested interrupt controller**
  - – Fast interrupt handling with multip[redacted]
  - – 32 vectors with 16 IRQ priority levels[redacted]
  - – 2 maskable FIQ sources
- ■ **Up to 48 I/O ports**
  - – 30/32/48 multifunctional bidirectional I/O li[redacted]
  - – Up to 14 ports with interrupt capability


TQFP64 10 x 1[redacted]


LFBGA64 8 x 8 x 1.7


LFBGA144 10 x 10 x 1.7

[redacted]tures, 2 outp[redacted]
[redacted]counter mode[redacted]
[redacted]nctions
[redacted]cations Interfaces
– 2 I^{2}C interfaces (1 mul[redacted]exed w[redacted]
[redacted]rial i[redacted]

Table 1. Device Summary

Features	STR710F Z1	STR710F Z2	STR711F R0	STR[redacted]	[redacted]	[redacted]	[redacted]TR[redacted] R[redacted]
Flash - Kbytes	128+16	256+16	64+16	[redacted]+16	256[redacted]	[redacted]	256[redacted]
RAM - Kbytes	32	64	16[redacted]	32	64	[redacted]	6[redacted]
Peripheral Functions	CAN, EMI, USB, 48 I/Os		USB, 30 I/Os			[redacted]	
Operating Voltage	3.0 to 3.6V[redacted]						
Operating Temp.	-40 to +85°C[redacted]						
Packages	**T**=TQFP14[redacted] x 20 **H**=LFBG[redacted]4 10 x10		**T**=TQFP64 10 x10 / **H**=LFBGA[redacted] x 1.7[redacted]				

Table of Contents

Note: For detailed information on the STR71xF Microcontroller memory, registers and peripherals. please refer to the STR71xF Reference Manual.

1 INTRODUCTION

This Preliminary Data provides the STR71x Ordering Information, Mechanical and Electrical Device Characteristics.

For complete information on the STR71xF Microcontroller memory, registers and peripherals. please refer to the STR71xF Reference Manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash Programming Reference Manual

For information on the ARM7TDMI core please refer to the ARM7TDMI Technical Reference Manual.

1.1 Overview

ARM® core with embedded Flash & RAM

The STR71xF series is a family of ARM-powered 32-bit Microcontrollers with embedded Flash and RAM. It combines the high performance ARM7TDMI CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage FLASH memory and high-speed RAM. The STR71xF family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs. The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

Package Choice: Low Pin-Count 64-pin or Feature-Rich 144-pin TQFP or BGA

The STR71xF family is available in 4 main versions.

The 144-pin versions have the full set of all features including CAN, USB and External Memory Interface.

- **STR710F:** 144-pin BGA or TQFP with CAN, USB and EMI

The three 64-pin versions (BGA or TQFP) do not include External Memory Interface.

- **STR715F:** 64-pin BGA or TQFP without CAN or USB
- **STR711F:** 64-pin BGA or TQFP with USB
- **STR712F:** 64-pin BGA or TQFP with CAN

High Speed Flash Memory

The Flash program memory is organized in two banks of 32-bit wide Burst Flash memories enabling true read-while-write (RWW) operation. Device Bank 0 is up to 256 Kbytes in size, typically for the application program code. Bank 1 is 16K bytes, typically used for storing data constants. Both banks are accessed by the CPU with zero wait states @ 33 MHz

Bank 0 memory endurance is 10K write/erase cycles and Bank 1 endurance is 100K write/ erase cycles. Data retention is 20 years at 55°C on both banks. The two banks can be accessed independently in read or write. Flash memory can be accessed in two modes:

- Burst mode: 64-bit wide memory access at up to 50 MHz.
- Direct 32-bit wide memory access for deterministic operation at up to 33 MHz.

The STR7 embedded Flash memory can be programmed using In-Circuit Programming or In-Application programming.

IAP (In-Application Programming): The IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.

ICP (In-Circuit Programming): The ICP is the ability to program the Flash memory of a microcontroller using JTAG protocol while the device is mounted on the user application board.

The Flash memory can be protected against different types of unwanted access (read/write/ erase). There are two types of protection:

- Sector Write Protection
- Flash Debug Protection (locks JTAG access)

Refer to the STR7 Flash Programming Reference manual for details.

Optional External Memory (STR710F)

The non-multiplexed 16-bit data/24-bit address bus available on the STR710F (144-pin) supports four 16-Mbyte banks of external memory. Wait states are programmable individually

for each bank allowing different memory types (Flash, EPROM, ROM, SRAM etc.) to be used to store programs or data.

Figure 1 shows the general block diagram of the device family.

Flexible Power Management

To minimize power consumption, you can program the STR71xF to switch to SLOW, WAIT, LPWAIT (low power wait), STOP or STANDBY mode depending on the current system activity in the application.

Flexible Clock Control

Two external clock sources can be used, a main clock and a 32 kHz backup clock. The embedded PLL allows the internal system clock (up to 66 MHz) to be generated from a main clock frequency of 16 MHz or less. The PLL output frequency can be programmed using a wide selection of multipliers and dividers. The microcontroller core, APB1 and APB2 peripherals are in separate clock domains and can be programmed to run at different frequencies during application runtime. The clock to each perhipheral is gated with an individual control bit to optimize power usage by turning off peripherals any time they are not required.

Voltage Regulators

The STR71xF requires an external 3.0-3.6V power supply. There are two internal Voltage Regulators for generating the 1.8V power supply for the core and peripherals. The main VR is switched off during low power operation.

Low Voltage Detectors

Each voltage regulator has an embedded LVD that monitors the internal 1.8V supply. If the voltage drops below a certain threshold, the LVD will reset the STR71xF.

On-Chip Peripherals

CAN Interface (STR710F and STR712F)

The CAN module is compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud.

USB Interface (STR710F and STR711F)

The full-speed USB interface is USB V2.0 compliant and provides up to 16 bidirectional/32 unidirectional endpoints, up to 12 Mb/s (full-speed), support for bulk transfer, isochronous transfers and USB Suspend/Resume functions.

Standard Timers

Each of the four timers have a 16-bit free-running counter with 7-bit prescaler

Three timers each provide up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency.

The fourth timer is not connected to the I/O ports. It can be used by the application software for general timing functions.

Realtime Clock (RTC)

The RTC provides a set of continuously running counters driven by the 32 kHz external crystal. The RTC can be used as a general timebase or clock/calendar/alarm function. When the STR71xF is in Standby mode the RTC can be kept running, powered by the low power voltage regulator and driven by the 32 kHz external crystal.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 625 kb/s.

Smart Card Interface

UART1 is configurable to function either as a general purpose UART or as an asynchronous Smart Card interface as defined by ISO 7816-3. It includes Smart Card clock generation and provides support features for synchronous cards.

Buffered Serial Peripheral Interfaces (BSPI)

Each of the two SPIs allow full duplex, synchronous communications with external devices, master or slave communication at up to 5.5Mb/s in Master mode and 4 Mb/s in Slave mode.

I^2C Interfaces

The two I^2C Interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 kHz) and 7 or 10-bit addressing modes.

One I^2C Interface is multiplexed with one SPI, so either 2xSPI+1x I^2C or 1xSPI+2x I^2C may be used at a time.

HDLC interface

The High Level Data Link Controller (HDLC) unit supports full duplex operation and NRZ, NRZI, FM0 or MANCHESTER protocols. It has an internal 8-bit baud rate generator.

A/D Converter

The Analog to Digital Converter, converts in single channel or up to 4 channels in single-shot or round robin mode. Resolution is 12-bit with a sampling frequency of up to 1 kHz. The input voltage range is 0-2.5V.

Watchdog

The 16-bit Watchdog Timer protects the application against hardware or software failures and ensures recovery by generating a reset.

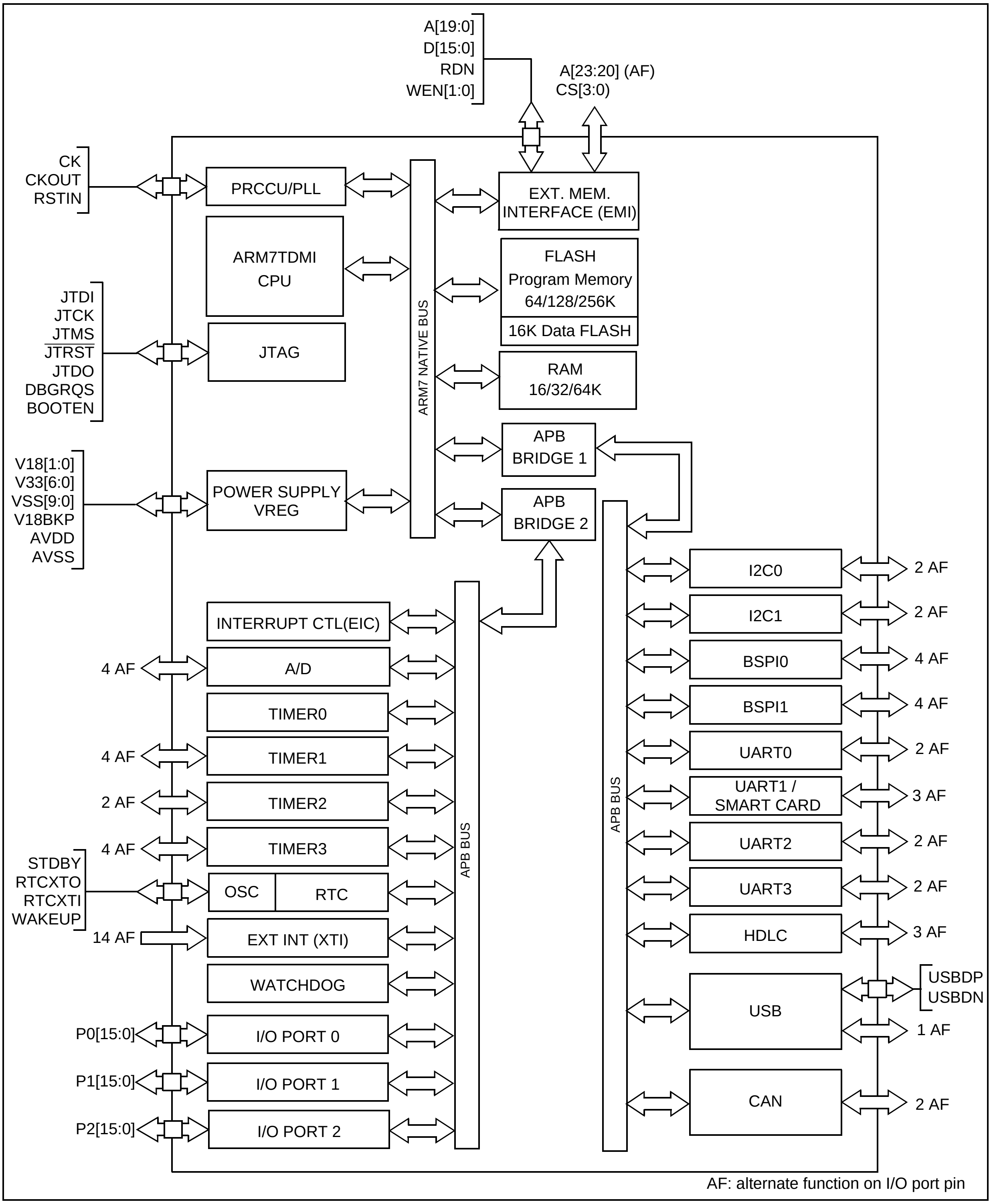
I/O Ports

The 48 I/O ports are programmable as Inputs or Outputs.

External Interrupts

Up to 14 external interrupts are available for application use or to wake-up the application from STOP mode.

Figure 1. STR71xF Block Diagram



1.2 Related Documentation

Available from www.arm.com:

ARM7TDMI Technical Reference Manual

Available from http://www.st.com:

STR71x Reference Manual

STR7 Flash Programming Reference Manual

AN1774 - STR71xF Software development getting started

AN1775 - STR71xF Hardware development getting started

AN1776 - STR71xF Enhanced Interrupt Controller

AN1777 - STR71xF Memory Mapping

AN1780 - Real Time Clock with STR71xF

AN1781 - Four 7 Segment Display Drive Using the STR71xF

The above is a selected list only, a full list STR71x application notes can be viewed at http://www.st.com.

1.3 Pin Description for 144-Pin Packages

Figure 2. STR710 TQFP Pinout

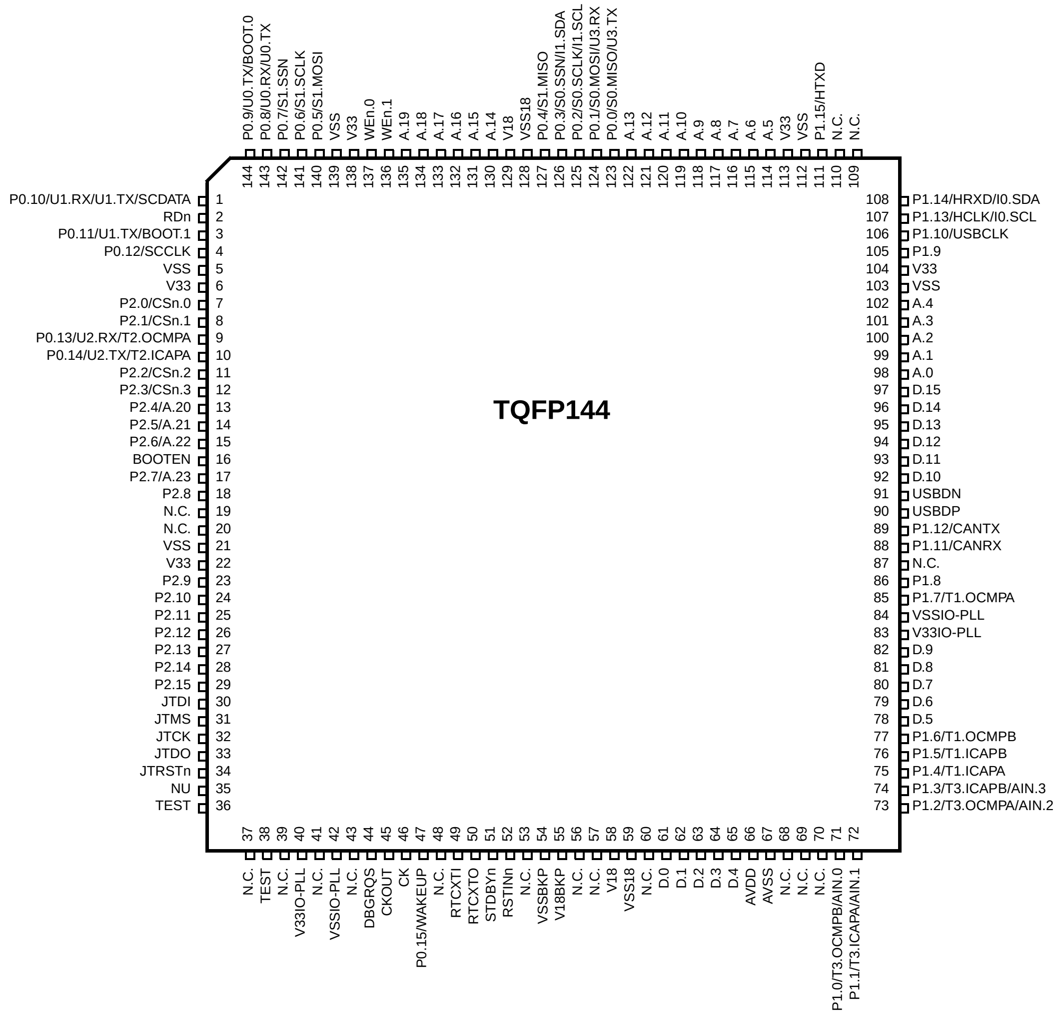


Table 2. **STR710 BGA Ball Connections**

	A	B	C	D	E	F	G	H	J	K	L	M
1	P0.10	P2.0	P2.1	VSS	P2.2	P2.6	BOOT EN	P2.12	P2.13	P2.15	JTDI	N.C.
2	VSS	RDn	P0.11	V33	P2.3	P2.8	P2.9	JTMS	JTRSTn	TEST	TEST	N.C.
3	V33	P0.9	P0.12	P0.13	P2.4	N.C.	P2.10	JTCK	NU	V33	N.C.	DBG RQS
4	P0.6	P0.7	P0.8	P0.14	P2.5	N.C.	P2.11	JTDO	CK	CKOUT	VSSIO-PLL	N.C.
5	A.19	WEn.1	WEn.0	P0.5	P2.7	VSS	P2.14	N.C.	RTCX-TO	RTCXTI	N.C.	P0.15
6	P0.3	A.15	A.16	A.17	A.18	V33	V18	N.C.	N.C.	V18BKP	VSS BKP	STDBYn
7	P0.2	P0.1	P0.4	VSS18	V18	A.14	D.12	D.1	D.0	nc	VSS18	RSTINn
8	A.9	A.10	A.11	A.13	P0.0	A.0	D.11	P1.12/ CANTX	N.C.	AVSS	D.3	D.2
9	VSS	V33	A.5	A.6	V33	D.15	D.10	P1.8	D.9	P1.0	N.C.	N.C.
10	A.8	N.C.	P1.15	P1.13	VSS	D.14	USBDN	P1.7	D.8	P1.5	P1.1	D.4
11	A.7	N.C.	P1.14	P1.10	A.2	D.13	USBDP	VSS	D.5	P1.4	P1.3	AVDD
12	A.12	A.4	A.3	P1.9	A.1	P1.11/ CANRX	N.C.	V33IO-PLL	P1.6	D.7	D.6	P1.2

Legend / Abbreviations for Table 3:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
T_T= TTL $0.8V_{DD}/2V$ with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8V / 2V

Port and control configuration:

– Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

– Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5V tolerant.

Table 3. STR710 Pin Description

Pin n° TQFP144	Pin n° BGA144	Pin Name	Type	Input Reset State[1)]	Input: Input Level	Input: interrupt	Output: Capability	Output: OD	Output: PP	Active in Stdby	Main function (after reset)	Alternate function	
1	A1	P0.10/U1.RX/ U1.TX/ SC.DATA	I/O	pd	C_T	X	4mA	T			Port 0.10	UART1: Receive Data input	UART1: Transmit data output.
												Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress	
2	B2	$\overline{RD}$	O						X		External Memory Interface: Active low read signal for external memory. It maps to the OE_N input of the external components.		
3	C2	P0.11/ BOOT.1/ U1.TX	I/O	pd	C_T		4mA	X	X		Port 0.11	Select Boot Configuration input	UART1: Transmit data output.
4	C3	P0.12/SC.CLK	I/O	pd	C_T		4mA	X	X		Port 0.12	Smartcard reference clock output	
5	D1	V_{SS}	S								Ground voltage for digital I/Os[4)]		
6	D2	V_{33}	S								Supply voltage for digital I/Os[4)]		
7	B1	P2.0/$\overline{CS}$.0	I/O	pu	C_T		8mA	X	X		Port 2.0	External Memory Interface: Select Memory Bank 0 output **Note:** This pin is forced to output mode at reset to allow boot from external memory	
8	C1	P2.1/$\overline{CS}$.1	I/O	pu[2)]	C_T		8mA	X	X		Port 2.1	External Memory Interface: Select Memory Bank 1 output	
9	D3	P0.13/U2.RX/ T2.OCMPA	I/O	pu	C_T	X	4mA	X	X		Port 0.13	UART2: Receive Data input	Timer2: Output Compare A output
10	D4	P0.14/U2.TX/ T2.ICAPA	I/O	pu	C_T		4mA	X	X		Port 0.14	UART2: Transmit data output	Timer2: Input Capture A input
11	E1	P2.2/$\overline{CS}$.2	I/O	pu[2)]	C_T		8mA	X	X		Port 2.2	External Memory Interface: Select Memory Bank 3 output	

Table 3. STR710 Pin Description

Pin n°		Pin Name	Type	Input Reset State[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function
TQFP144	BGA144				Input Level	interrupt	Capability	OD	PP			
12	E2	P2.3/$\overline{CS}$.3	I/O	pu[2]	C_T		8mA	X	X		Port 2.3	External Memory Interface: Select Memory Bank 4 output
13	E3	P2.4/A.20	I/O	pd[3]	C_T		8mA	X	X		Port 2.4	
14	E4	P2.5/A.21	I/O	pd[3]	C_T		8mA	X	X		Port 2.5	External Memory Interface: address bus
15	F1	P2.6/A.22	I/O	pd[3]	C_T		8mA	X	X		Port 2.6	
16	G1	BOOTEN	I		C_T						Boot control input. Enables sampling of BOOT[1:0] pins	
17	E5	P2.7/A.23	I/O	pd[3]	C_T		8mA	X	X		Port 2.7	External Memory Interface: address bus
18	F2	P2.8	I/O	pu	C_T	X	4mA	X	X		Port 2.8	External interrupt INT2
19	F3	N.C.									Not connected (not bonded)	
20	F4	N.C.									Not connected (not bonded)	
21	F5	V_{SS}	S								Ground voltage for digital I/Os[4]	
22	F6	V_{33}	S								Supply voltage for digital I/Os[4]	
23	G2	P2.9	I/O	pu	C_T	X	4mA	X	X		Port 2.9	External interrupt INT3
24	G3	P2.10	I/O	pu	C_T	X	4mA	X	X		Port 2.10	External interrupt INT4
25	G4	P2.11	I/O	pu	C_T	X	4mA	X	X		Port 2.11	External interrupt INT5
26	H1	P2.12	I/O	pu	C_T		4mA	X	X		Port 2.12	
27	J1	P2.13	I/O	pu	C_T		4mA	X	X		Port 2.13	
28	G5	P2.14	I/O	pu	C_T		4mA	X	X		Port 2.14	
29	K1	P2.15	I/O	pu	C_T		4mA	X	X		Port 2.15	
30	L1	JTDI	I		T_T						JTAG Data input. External pull-up required.	
31	H2	JTMS	I		T_T						JTAG Mode Selection Input. External pull-up required.	
32	H3	JTCK	I		C						JTAG Clock Input. External pull-up or pull-down required.	
33	H4	JTDO	O				8mA		X		JTAG Data output. **Note:** Reset state = HiZ.	
34	J2	$\overline{JTRST}$	I		T_T						JTAG Reset Input. External pull-up required.	
35	J3	NU									Reserved, must be forced to ground.	
36	K2	TEST									Reserved, must be forced to ground.	
37	M1	N.C.									Not connected (not bonded)	
38	L2	TEST									Reserved, must be forced to ground.	
39	L3	N.C.									Not connected (not bonded)	

Table 3. STR710 Pin Description

Pin n°		Pin Name	Type	Input Reset State[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function
TQFP144	BGA144				Input Level	interrupt	Capability	OD	PP			
40	K3	$V_{33IO\text{-}PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference	
41	M4	N.C.									Not connected (not bonded)	
42	L4	$V_{SSIO\text{-}PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[4)]	
43	M2	N.C.									Not connected (not bonded)	
44	M3	DBGRQS	I		C_T						Debug Mode request input (active high)	
45	K4	CKOUT	O				8mA		X		Clock output (f_{PCLK2}) **Note:** Enabled by CKDIS register in APB Bridge 2	
46	J4	CK	I		C						Reference clock input	
47	M5	P0.15/WAKE-UP	I	pu	T_T	X	4mA			X	Port 0.15	Wakeup from Standby mode input.
48	L5	N.C.									Not connected (not bonded)	
49	K5	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit	
50	J5	RTCXTO									Output of 32 kHz oscillator amplifier circuit	
51	M6	$\overline{\text{STDBY}}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby	
52	M7	$\overline{\text{RSTIN}}$	I		C_T					X	Reset input	
53	H5	N.C.									Not connected (not bonded)	
54	L6	V_{SSBKP}			S					X	Stabilisation for low power voltage regulator.	
55	K6	V_{18BKP}			S					X	Stabilisation for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See Figure 5. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.	
56	J6	N.C.									Not connected (not bonded)	
57	H6	N.C.									Not connected (not bonded)	
58	G6	V_{18}	S								Stabilisation for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See Figure 5.	
59	L7	V_{SS18}	S								Stabilisation for main voltage regulator.	
60	K7	N.C.									Not connected (not bonded)	

Table 3. STR710 Pin Description

Pin n°		Pin Name	Type	Input Reset State[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
TQFP144	BGA144				Input Level	interrupt	Capability	OD	PP				
61	J7	D.0	I/O				8mA				External Memory Interface: data bus		
62	H7	D.1	I/O				8mA				External Memory Interface: data bus		
63	M8	D.2	I/O				8mA				External Memory Interface: data bus		
64	L8	D.3	I/O				8mA				External Memory Interface: data bus		
65	M10	D.4	I/O				8mA				External Memory Interface: data bus		
66	M11	V_{DDA}	S								Supply voltage for A/D Converter		
67	K8	V_{SSA}	S								Ground voltage for A/D Converter		
68	J8	N.C.									Not connected (not bonded)		
69	M9	N.C.									Not connected (not bonded)		
70	L9	N.C.									Not connected (not bonded)		
71	K9	P1.0/T3.OC-MPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
72	L10	P1.1/T3.ICA-PA/T3.EXT-CLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
73	M12	P1.2/T3.OCM-PA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
74	L11	P1.3/ T3.ICAPB/ AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
75	K11	P1.4/T1.ICA-PA/T1.EXT-CLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input
76	K10	P1.5/ T1.ICAPB	I/O	pu	C_T		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
77	J12	P1.6/T1.OC-MPB	I/O	pu	C_T		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
78	J11	D.5	I/O				8mA				External Memory Interface: data bus		
79	L12	D.6	I/O				8mA				External Memory Interface: data bus		
80	K12	D.7	I/O				8mA				External Memory Interface: data bus		
81	J10	D.8	I/O				8mA				External Memory Interface: data bus		
82	J9	D.9	I/O				8mA				External Memory Interface: data bus		
83	H12	$V_{33IO\text{-}PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[4]		
84	H11	$V_{SSIO\text{-}PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[4]		
85	H10	P1.7/T1.OCM-PA	I/O	pu	C_T		4mA	X	X		Port 1.7	Timer 1: Output Compare A	
86	H9	P1.8	I/O	pd	C_T		4mA	X	X		Port 1.8		
87	G12	N.C.									Not connected (not bonded)		

Table 3. STR710 Pin Description

Pin n°		Pin Name	Type	Input Reset State[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
TQFP144	BGA144				Input Level	interrupt	Capability	OD	PP				
88	F12	P1.11/CANRX	I/O	pu	C_T	X	4mA	X	X		Port 1.11	CAN: receive data input **Note:** On STR710 and STR712 only	
89	H8	P1.12/CANTX	I/O	pu	C_T	X	4mA	X	X		Port 1.12	CAN: Transmit data output **Note:** On STR710 and STR712 only	
90	G11	USBDP	I/O		C_T						USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to V_{33} to maintain a high level.		
91	G10	USBDN	I/O		C_T						USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only.		
92	G9	D.10	I/O				8mA				External Memory Interface: data bus		
93	G8	D.11	I/O				8mA						
94	G7	D.12	I/O				8mA						
95	F11	D.13	I/O				8mA						
96	F10	D.14	I/O				8mA						
97	F9	D.15	I/O				8mA						
98	F8	A.0	O				8mA				External Memory Interface: address bus		
99	E12	A.1	O				8mA						
100	E11	A.2	O				8mA						
101	C12	A.3	O				8mA						
102	B12	A.4	O				8mA						
103	E10	V_{SS}	S								Ground voltage for digital I/O circuitry[4)]		
104	E9	V_{33}	S								Supply voltage for digital I/O circuitry[4)]		
105	D12	P1.9	I/O	pd	C_T		4mA	X	X		Port 1.9		
106	D11	P1.10/USB-CLK	I/O	pu	C/T		4mA	X	X		Port 1.10	USB: 48 MHZ clock input	
107	D10	P1.13/HCLK/I0.SCL	I/O	pu	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
108	C11	P1.14/HRXD/I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
109	B11	N.C.									Not connected (not bonded)		
110	B10	N.C.									Not connected (not bonded)		
111	C10	P1.15/HTXD	I/O	pu	C_T	X	4mA	X	X		Port 1.15	HDLC: Transmit data output	
112	A9	V_{SS}	S								Ground voltage for digital I/O circuitry[4)]		
113	B9	V_{33}	S								Supply voltage for digital I/O circuitry[4)]		

Table 3. STR710 Pin Description

Pin n° TQFP144	Pin n° BGA144	Pin Name	Type	Input Reset State[1)]	Input: Input Level	Input: interrupt	Output: Capability	Output: OD	Output: PP	Active in Stdby	Main function (after reset)	Alternate function
114	C9	A.5	O				8mA					
115	D9	A.6	O				8mA					
116	A11	A.7	O				8mA					
117	A10	A.8	O				8mA					
118	A8	A.9	O				8mA				External Memory Interface: address bus	
119	B8	A.10	O				8mA					
120	C8	A.11	O				8mA					
121	A12	A.12	O				8mA					
122	D8	A.13	O				8mA					
123	E8	P0.0/S0.MISO/ U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/ Slave out data | UART3 Transmit data output **Note:** Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.
124	B7	P0.1/S0.MOSI/ U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data | UART3: Receive Data input **Note:** Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.
125	A7	P0.2/ S0.SCLK/ I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock | I2C1: Serial clock **Note:** Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.
126	A6	P0.3/S0.$\overline{SS}$/ I1.SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low. | I2C1: Serial Data **Note:** Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.
127	C7	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data
128	D7	V_{SS18}	S								Stabilisation for main voltage regulator.	
129	E7	V_{18}	S								Stabilisation for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See Figure 5.	
130	F7	A.14	O				8mA					
131	B6	A.15	O				8mA					
132	C6	A.16	O				8mA				External Memory Interface: address bus	
133	D6	A.17	O				8mA					
134	E6	A.18	O				8mA					
135	A5	A.19	O				8mA					

Table 3. STR710 Pin Description

Pin n° TQFP144	Pin n° BGA144	Pin Name	Type	Input Reset State[1)]	Input: Input Level	Input: interrupt	Output: Capability	Output: OD	Output: PP	Active in Stdby	Main function (after reset)	Alternate function	
136	B5	$\overline{WE}$.1	O				8mA				External Memory Interface: active low MSB write enable output		
137	C5	$\overline{WE}$.0	O				8mA				External Memory Interface: active low LSB write enable output		
138	A3	V_{33}	S								Supply voltage for digital I/Os[4)]		
139	A2	V_{SS}	S								Ground voltage for digital I/Os[4)]		
140	D5	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
141	A4	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
142	B4	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	
143	C4	P0.8/U0.RX/ U0.TX	I/O	pd	C_T	X	4mA	T			Port 0.8	UART0: Receive Data input	UART0: Transmit data output.
											Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress		
144	B3	P0.9/U0.TX/ BOOT.0	I/O	pd	C_T		4mA	X	X		Port 0.9	Select Boot Configuration input	UART0: Transmit data output

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to Table 7, "Port Bit Configuration Table," on page 26. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset

2. In reset state, these pins configured as Input PU/PD with weak pull-up enabled. They must be configured by software as Alternate Function (see Table 7, "Port Bit Configuration Table," on page 26) to be used by the External Memory Interface.

3. In reset state, these pins configured as Input PU/PD with weak pull-down enabled to output Address 0x0000 0000 using the External Memory Interface. To access memory banks greater than 1Mbyte, they need to be configured by software as Alternate Function (see Table 7, "Port Bit Configuration Table," on page 26).

4. $V_{33IO-PLL}$ and V_{33} are internally connected. $V_{SSIO-PLL}$ and V_{SS} are internally connected.

Figure 4. STR711F TQFP64 Pinout

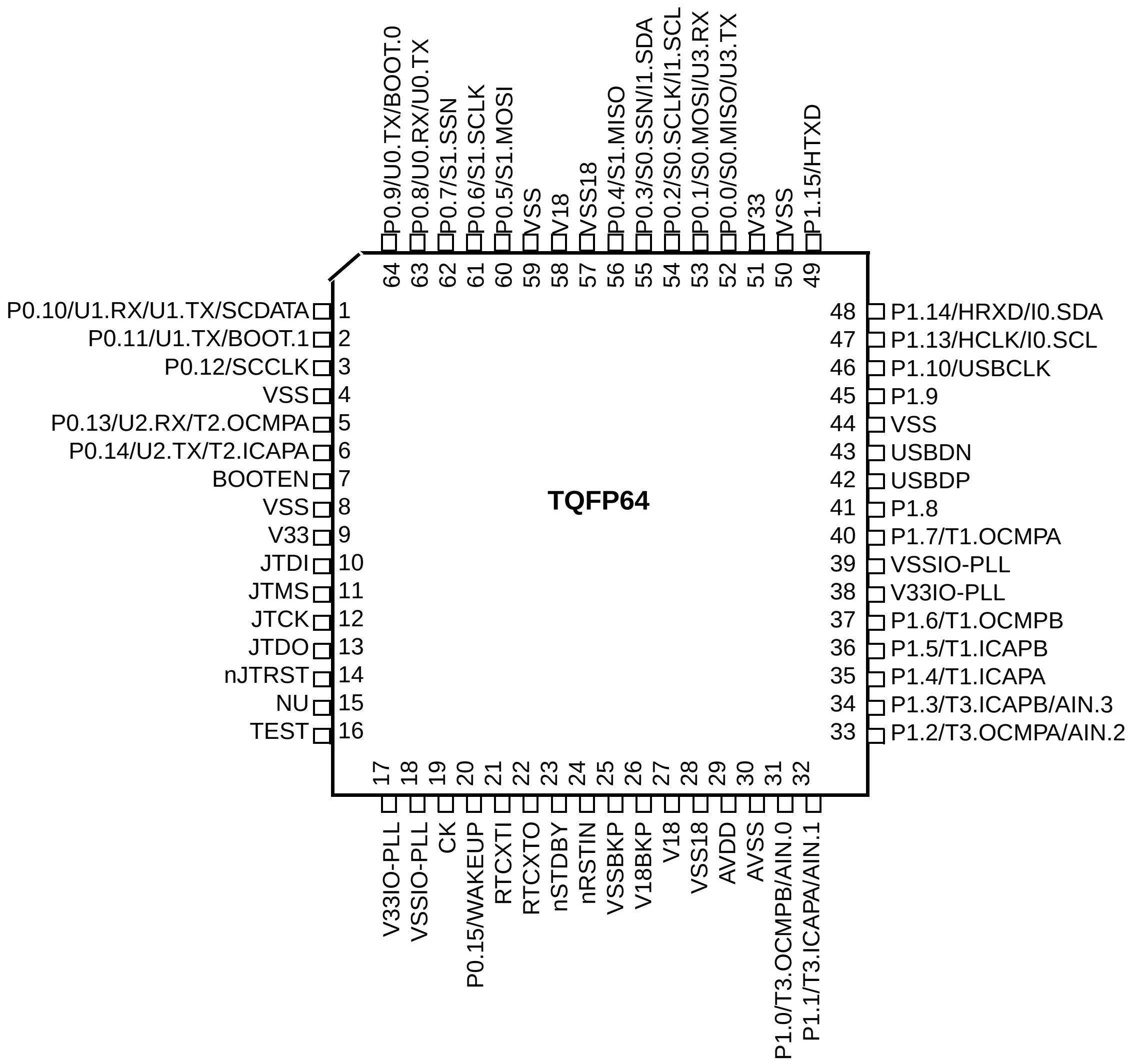


Table 4. **STR711F BGA Ball Connections**

	A	B	C	D	E	F	G	H
1	P0.10	P0.11	P0.12	P0.14	V33	JTCK	TEST	V33IO-PLL
2	P0.9	VSS	P0.13	VSS	JTMS	JTRSTn	P0.15	VSSIO-PLL
3	P0.5	P0.7	BOOTEN	JTDI	NU	STDBYn	RTCXTI	CK
4	VSS18	VSS	P0.8	JTDO	AVDD	V18BKP	RSTINn	RTCXTO
5	P0.2	P0.4	V18	P0.6	P1.9	P1.0	V18	VSSBKP
6	V33	P0.1	P0.3	P1.13	USBDP	VSSIO-PLL	AVSS	VSS18
7	VSS	P0.0	P1.10	USBDN	P1.7	P1.6	P1.5	P1.1
8	P1.15	P1.14	VSS	P1.8	V33IO-PLL	P1.4	P1.3	P1.2

Table 5. **STR712F/715F BGA Ball Connections**

	A	B	C	D	E	F	G	H
1	P0.10	P0.11	P0.12	P0.14	V33	JTCK	TEST	V33IO-PLL
2	P0.9	VSS	P0.13	VSS	JTMS	JTRSTn	P0.15	VSSIO-PLL
3	P0.5	P0.7	BOOTEN	JTDI	NU	STDBYn	RTCXTI	CK
4	VSS18	VSS	P0.8	JTDO	AVDD	V18BKP	RSTINn	RTCXTO
5	P0.2	P0.4	V18	P0.6	P1.9	P1.0	V18	VSSBKP
6	V33	P0.1	P0.3	P1.13	P1.11/ CANRX[1)]	VSSIO-PLL	AVSS	VSS18
7	VSS	P0.0	P1.10	P1.12/ CANTX[1)]	P1.7	P1.6	P1.5	P1.1
8	P1.15	P1.14	VSS	P1.8	V33IO-PLL	P1.4	P1.3	P1.2

[1)]CANTX and CANRX in STR712F only, in STR715F they are general purpose I/Os.

Legend / Abbreviations for Table 3:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS 0.8V / 2V with input trigger
T_T= TTL $0.3V_{DD}/0.7V_{DD}$ with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8V / 2V

Port and control configuration:

– Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

– Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5V tolerant.

Table 6. STR711/STR712/STR715 Pin Description

Pin n°		Pin Name	Type	Input Reset State[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
TQFP64	BGA64				Input Level	interrupt	Capability	OD	PP				
1	A1	P0.10/U1.RX/U1.TX/SC.DATA	I/O	pd	C_T	X	4mA	T			Port 0.10	UART1: Receive Data input	UART1: Transmit data output.
												Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress	
2	B1	P0.11/BOOT.1/U1.TX	I/O	pd	C_T		4mA	X	X		Port 0.11	Select Boot Configuration input	UART1: Transmit data output.
3	C1	P0.12/SC.CLK	I/O	pd	C_T		4mA				Port 0.12	Smartcard reference clock output	
4	B2	V_{SS}	S								Ground voltage for digital I/Os[2]		
5	C2	P0.13/U2.RX/T2.OCMPA	I/O	pu	C_T	X	4mA	X	X		Port 0.13	UART2: Receive Data input	Timer2: Output Compare A output
6	D1	P0.14/U2.TX/T2.ICAPA	I/O	pu	C_T		4mA	X	X		Port 0.14	UART2: Transmit data output	Timer2: Input Capture A input
7	C3	BOOTEN	I		C_T						Boot control input. Enables sampling of BOOT[1:0] pins		
8	D2	V_{SS}	S								Ground voltage for digital I/Os[2]		
9	E1	V_{33}	S								Supply voltage for digital I/Os[2]		
10	D3	JTDI	I		T_T						JTAG Data input. External pull-up required.		
11	E2	JTMS	I		T_T						JTAG Mode Selection Input. External pull-up required.		
12	F1	JTCK	I		C						JTAG Clock Input. External pull-up or pull-down required.		
13	D4	JTDO	O				8mA		X		JTAG Data output. **Note:** Reset state = HiZ.		
14	F2	$\overline{JTRST}$	I		T_T						JTAG Reset Input. External pull-up required.		
15	E3	NU									Reserved, must be forced to ground.		

Table 6. STR711/STR712/STR715 Pin Description

Pin n° TQFP64	Pin n° BGA64	Pin Name	Type	Input Reset State[1)]	Input: Input Level	Input: interrupt	Output: Capability	Output: OD	Output: PP	Active in Stdby	Main function (after reset)	Alternate function	
16	G1	TEST									Reserved, must be forced to ground.		
17	H1	$V_{33IO\text{-}PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[2)]		
18	H2	$V_{SSIO\text{-}PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[2)]		
19	H3	CK	I		C						Reference clock input		
20	G2	P0.15/WAKE-UP	I	pu	T_T	X	4mA			X	Port 0.15	Wakeup from Standby mode input.	
21	G3	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit		
22	H4	RTCXTO									Output of 32 kHz oscillator amplifier circuit		
23	F3	$\overline{STDBY}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby		
24	G4	$\overline{RSTIN}$	I		C_T					X	Reset input		
25	H5	V_{SSBKP}			S					X	Stabilisation for low power voltage regulator.		
26	F4	V_{18BKP}			S					X	Stabilisation for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See Figure 5. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.		
27	G5	V_{18}	S								Stabilisation for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See Figure 5.		
28	H6	V_{SS18}	S								Stabilisation for main voltage regulator.		
29	E4	V_{DDA}	S								Supply voltage for A/D Converter		
30	G6	V_{SSA}	S								Ground voltage for A/D Converter		
31	F5	P1.0/T3.OC-MPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
32	H7	P1.1/T3.ICA-PA/T3.EXT-CLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
33	H8	P1.2/T3.OCM-PA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
34	G8	P1.3/ T3.ICAPB/ AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3

Table 6. STR711/STR712/STR715 Pin Description

Pin n°		Pin Name	Type	Input Reset State[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
TQFP64	BGA64				Input Level	interrupt	Capability	OD	PP				
35	F8	P1.4/T1.ICA-PA/T1.EXT-CLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input
36	G7	P1.5/ T1.ICAPB	I/O	pu	C_T		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
37	F7	P1.6/T1.OC-MPB	I/O	pu	C_T		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
38	E8	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[2]		
39	F6	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[2]		
40	E7	P1.7/T1.OCM-PA	I/O	pu	C_T		4mA	X	X		Port 1.7	Timer 1: Output Compare A	
41	D8	P1.8	I/O	pd	C_T		4mA	X	X		Port 1.8		
42	E6	P1.11/CANRX	I/O	pu	C_T	X	4mA	X	X		Port 1.11	CAN: receive data input **Note:** On STR710 and STR712 only	
43	D7	P1.12/CANTX	I/O	pu	C_T	X	4mA	X	X		Port 1.12	CAN: Transmit data output **Note:** On STR710 and STR712 only	
42	E6	USBDP	I/O		C_T						USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to V_{33} to maintain a high level.		
43	D7	USBDN	I/O		C_T						USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only.		
44	C8	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
45	E5	P1.9	I/O	pd	C_T		4mA	X	X		Port 1.9		
46	C7	P1.10/USB-CLK	I/O	pu	C/T		4mA	X	X		Port 1.10	USB: 48 MHZ clock input	
47	D6	P1.13/HCLK/ I0.SCL	I/O	pu	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
48	B8	P1.14/HRXD/ I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
49	A8	P1.15/HTXD	I/O	pu	C_T	X	4mA	X	X		Port 1.15	HDLC: Transmit data output	
50	A7	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
51	A6	V_{33}	S								Supply voltage for digital I/O circuitry[2]		
52	B7	P0.0/S0.MISO/ U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/ Slave out data **Note:** Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	UART3 Transmit data output

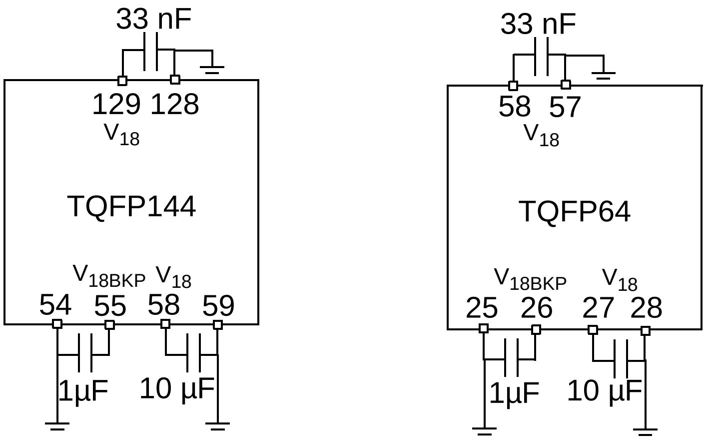
53	B6	P0.1/S0.MOSI/ U3.RX	I/O	pu	C_T	X	4mA	X	X	Port 0.1	BSPI0: Master out/Slave in data **Note:** Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	UART3: Receive Data input
54	A5	P0.2/ S0.SCLK/ I1.SCL	I/O	pu	C_T	X	4mA	X	X	Port 0.2	BSPI0: Serial Clock **Note:** Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	I2C1: Serial clock
55	C6	P0.3/S0.$\overline{SS}$/ I1.SDA	I/O	pu	C_T		4mA	X	X	Port 0.3	SPI0: Slave Select input active low. **Note:** Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	I2C1: Serial Data
56	B5	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X	Port 0.4	SPI1: Master in/Slave out data	
57	A4	V_{SS18}	S							Stabilisation for main voltage regulator.		
58	C5	V_{18}	S							Stabilisation for main voltage regulator. Requires external capacitorabi(s of at leamust)-6.10µF + 33nFstV		

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to Table 7, “Port Bit Configuration Table,” on page 26. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset

2. $V_{33IO-PLL}$ and V_{33} are internally connected. $V_{SSIO-PLL}$ and V_{SS} are internally connected.

1.5 External Connections

Figure 5. Recommended External Connection of V_{18} and V_{18BKP} pins



1.6 I/O Port Configuration

Table 7. Port Bit Configuration Table

Port Configuration Registers (bit)	**Values**							
PC0(n)	0	1	0	1	0	1	0	1
PC1(n)	0	0	1	1	0	0	1	1
PC2(n)	0	0	0	0	1	1	1	1
Configuration	HiZ/AIN	IN	IN	IPUPD	OUT	OUT	AF	AF
Output	TRI	TRI	TRI	WP	OD	PP	OD	PP
Input	AIN	TTL	CMOS	CMOS	N.A.	N.A.	CMOS	CMOS

Notes:

AF: Alternate Function
AIN: Analog Input
IPUPD: Input Pull Up /Pull Down
CMOS: CMOS Input levels
HiZ: High impedance
IN: Input
N.A. not applicable. In Output mode, a read access to the port gets the output latch value).

OD: Open Drain
OUT: Output
PP: Push-Pull
TRI: Tristate
TTL: TTL Input levels
WP: Weak Push-Pull

1.7 Memory Mapping

Figure 6. Memory Map

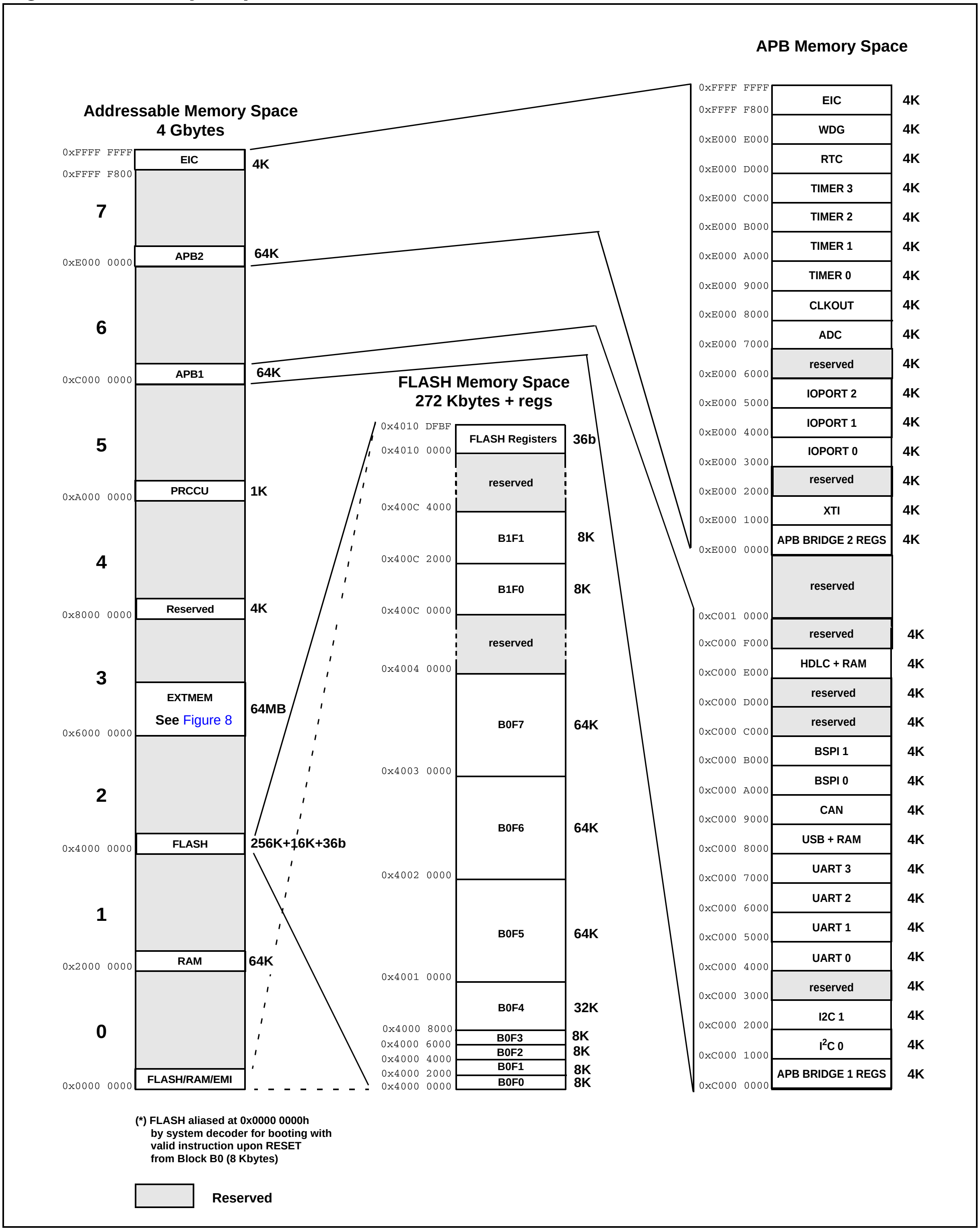


Figure 7. Mapping of Flash Memory Versions

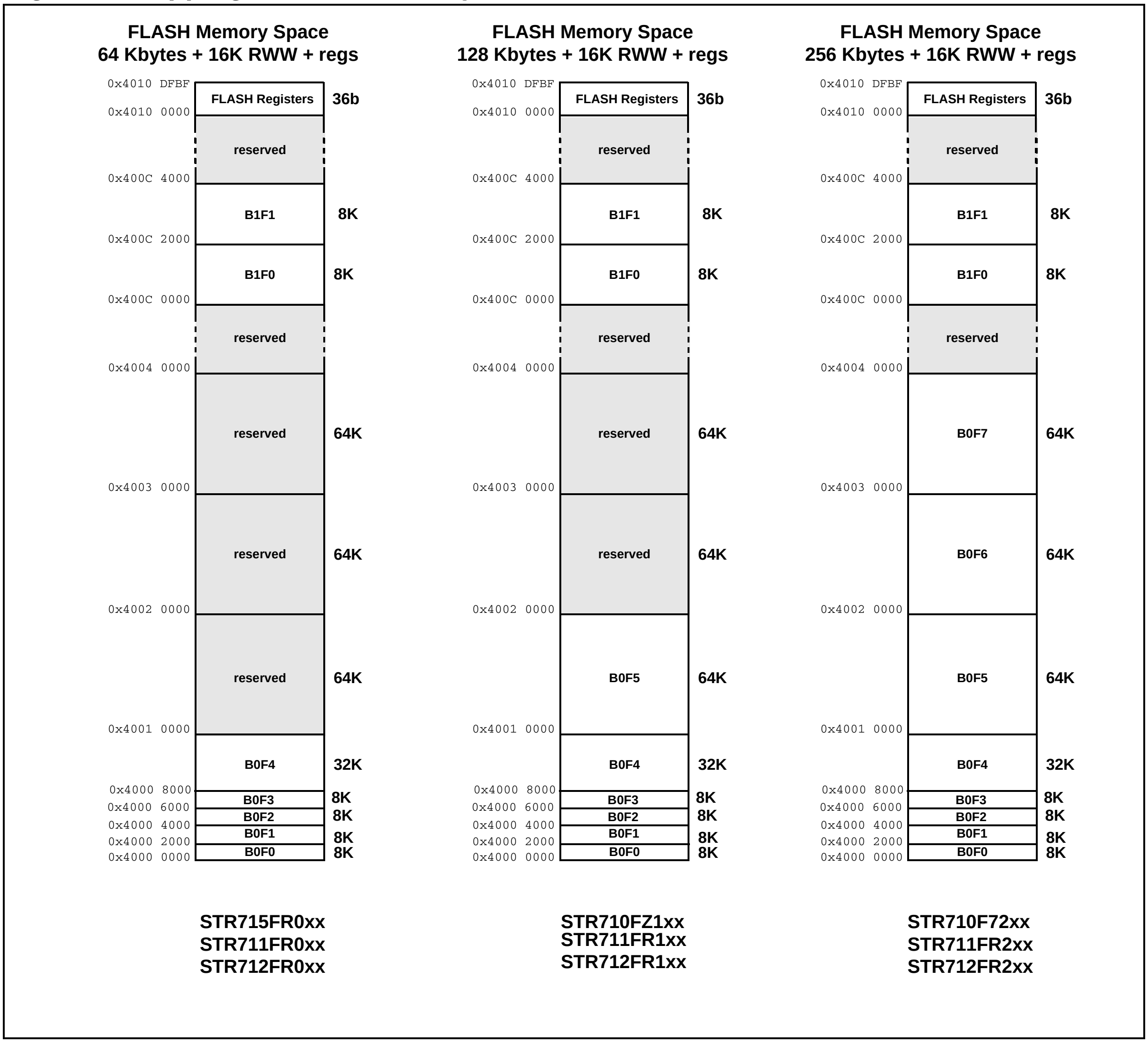
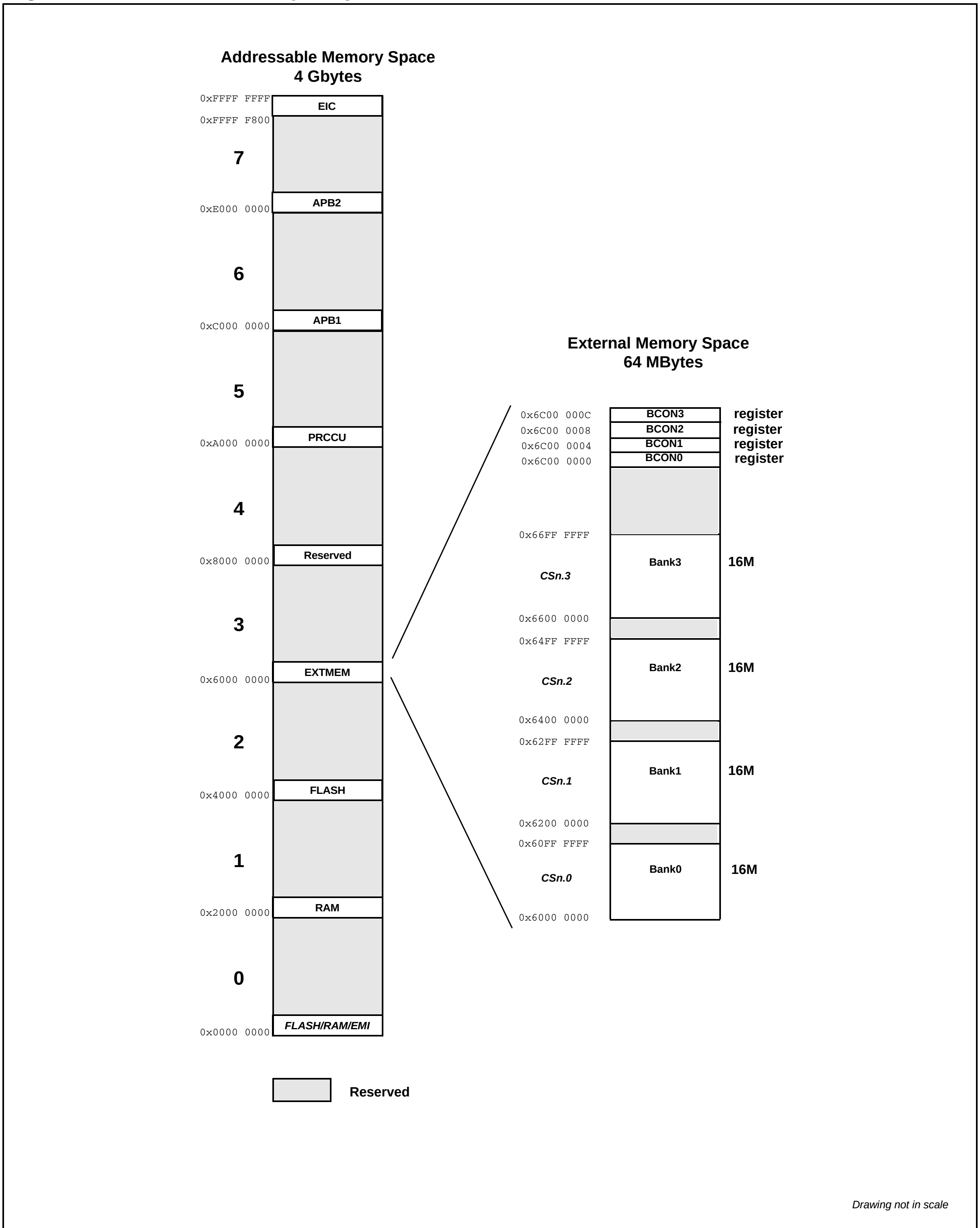


Table 8. RAM Memory Mapping

Part Number	RAM Size	Start Address	End Address
STR715FR0xx STR711FR0xx STR712FR0xx	16 Kbytes	0x2000 0000	0x2000 3FFF
STR710FZ1xx STR711FR1xx STR712FR1xx	32 Kbytes	0x2000 0000	0x2000 7FFF
STR710FR2xx STR711FR2xx STR712FR2xx	64 Kbytes	0x2000 0000	0x2000 FFFF

Figure 8. External Memory Map



2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

For proper operation, it is recommended that V_{IN} and V_O be higher than V_{SS} and lower than V_{33}. Reliability is enhanced if unused inputs are connected to an appropriate logic voltage level (V_{33} or V_{SS}).

Table 9. Absolute Maximum Ratings.

Symbol	Parameter	Value		Unit
		Min	**Max**	
V_{33}	Voltage on V_{33} with respect to ground (V_{SS})	-0.3	+4.0	V
$V_{33IO-PLL}$	Voltage on $V_{33IO-PLL}$ with respect to ground (V_{SS})	-0.3	+4.0	V
V_{18}	Voltage on V_{18} with respect to ground (V_{SS})	-0.3	+2.0	V
V_{18BKP}	Voltage on V_{18BKP} with respect to ground (V_{SS})	-0.3	+2.0	V
AV_{DD}	Voltage on AV_{DD} pin with respect to ground (V_{SS})	-0.3	+4.0	V
AV_{SS}	Voltage on AV_{SS} with respect to ground (V_{SS})	-0.1	V_{33} + 0.1	V
V_{IN}	Voltage on true open drain pin (P0.10) with respect to ground (V_{SS})	-0.3	+5.5	V
	Voltage on any other pin with respect to ground (V_{SS})	-0.3	+4.0	
I_{OV}	Input current on any pin during overload condition	-10	+10	mA
I_{TDV}	Absolute sum of all input currents during overload condition		|200|	mA
T_{ST}	Storage Temperature	–55	+150	°C
ESD	ESD Susceptibility (Human Body Model)	2000		V

Note *Stresses exceeding above listed recommended “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN}>V_{33}$ or $V_{IN}<V_{SS}$) the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.*

2.2 Operating Conditions

Symbol	Parameter	Value		Unit
		Min	Max	
V_{33}	Digital Supply Voltage for I/O circuitry	3.0	3.6	V
$V_{33IO\text{-}PLL}$	Digital Supply Voltage for I/O circuitry and for PLL reference	3.0	3.6	V
V_{18BKP}	External Supply Voltage for Backup block (Voltage Regulator off)	1.4	1.8	V
AV_{DD}	Analog Supply Voltage for the A/D converter	V_{33}	V_{33}	V
AV_{SS}	Ground Voltage for the A/D converter	V_{SS}	V_{SS}	V
T_A	Ambient temperature under bias	–40	+85	°C
T_J	Junction temperature under bias	–40	+105	°C

Note *RAM data retention is guaranteed with V_{33} not below 2.7 Volt, with the device in low power mode (STOP or WAIT).*

2.3 LVD Electrical Characteristics

V_{33} = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 10. LVD Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
V_{IT}	LVD Threshold	Main and LP LVDs		1.3	1.45	V

2.4 DC Electrical Characteristics

V_{33} = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 11. DC Electrical Characteristics

Symbol	Parameter	Comment	Value			Unit
			Min	Typ	Max	
V_{IH}	Input High Level CMOS	With or w/o hysteresis	$0.7V_{33}$			V
	Input High Level	P0.15 (WAKEUP) only	1.8			V
V_{IL}	Input Low Level CMOS	With or w/o hysteresis			$0.3V_{33}$	V
	Input Low Level	P0.15 (WAKEUP) only			0.7	V
V_{HYS}	Input Hysteresis CMOS Schmitt Trigger		0.4	0.8	1.2	V
	Input Hysteresis Schmitt Trigger	P0.15 (WAKEUP) only	0.3	0.5		V
V_{OH}	Output High Level High Current Pins	Push Pull, I_{OH}= 8mA	V_{33} – 0.8			V
	Output High Level Standard Current Pins	Push Pull, I_{OH}= 4mA	V_{33} – 0.8			V
V_{OL}	Output Low Level High Current Pins	Push Pull, I_{OL}= 8mA			0.4	V
	Output Low Level Standard Current Pins	Push Pull, I_{OL}= 4mA			0.4	V
R_{WPU}	Weak Pull-Up Resistor	Measured at $0.5V_{33}$		100		kΩ
R_{WPD}	Weak Pull-Down Resistor	Measured at $0.5V_{33}$		100		kΩ

2.5 AC Electrical Characteristics

V_{33} = 3.0 to 3.6V, T_A = 27 °C unless otherwise specified.

Table 12. Power consumption

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{DDRUN}	RUN Mode current	MCLK=50 MHz,		See Table 13	100	mA
I_{DDWAIT}	WAIT Mode current	1 MHz System Clock				mA
$I_{DDLPWAIT}$	LPWAIT Mode current	32 kHz System Clock				µA
I_{DDSTP}	STOP Mode current	Main VReg off, Flash in Power-Down				µA
I_{DDSB}	STANDBY Mode current	LP VReg and 32kHz Osc on			30	µA
		LP VReg, LVD, 32kHz Osc bypassed			10	µA

Notes:

– I_{DDRUN} is the power consumption when the application is using the full performance of the core (running at the maximum frequency).

– I_{DDWAIT} is the power consumption with PLLs off, VReg and Flash on. This guarantees the minimum interrupt response time.

– $I_{DDLPWAIT}$ is the power consumption with PLLs, Main VReg and Flash off.

Table 13. Power consumption

Symbol	Parameter		Conditions	Typical current on V33	Unit
I_{DDRUN}	RUN mode current from RAM	All periphs ON	MCLK = 16 MHz, PCLK = FCLK = 16 MHz	23	mA
			MCLK = 32 MHz, PCLK = FCLK = 32 MHz	40	
			MCLK = 48 MHz, PCLK = FCLK = 24 MHz	50	
			MCLK = 64 MHz, PCLK = FCLK = 32 MHz	63	
		All periphs OFF	MCLK = 16 MHz	16	
			MCLK = 32 MHz	26	
			MCLK = 48 MHz	39	
			MCLK = 64 MHz	48	
	RUN mode current from FLASH	All periphs ON	MCLK = 16 MHz, PCLK = FCLK = 16MHz	27	
			MCLK = 32 MHz, PCLK = FCLK = 32 MHz	47	
			MCLK = 48 MHz, PCLK = FCLK = 24 MHz	62	
		All periphs OFF	MCLK = 16 MHz	21	
			MCLK = 32 MHz	36	
			MCLK = 48 MHz	53	
I_{DDSLOW}	SLOW mode current		MCLK = CK_AF (32KHz), MVR off	2.2	
I_{DDWAIT}	WAIT mode current (all periphs ON)		PCLK = FCLK = 1 MHz	13	
$I_{DDLPWAIT}$	LPWAIT mode current		CK_AF(32KHz) ,Main VReg off, FLASH in power-down	76	uA
I_{DDSTOP}	STOP mode current		Main VReg off, FLASH in power down, RTC on	49	
			Main VReg off, FLASH in power down, RTC off	46	
I_{DDSB}	STANDBY mode current		LP VReg on, LVD on, RTC on	14	
			LP VReg off (ext 1.8V on V_{18BKP}), LVD on, RTC on	9	
			LP VReg off (ext1.8V on V_{18BKP}), LVD off, RTC on	5	
			LP VReg off (ext 1.8V on V_{18BKP}), LVD off, RTC off	1	

2.6 System Clock Characteristics

V_{33} = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 14. System Clock Characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{MCLK}	CPU Frequency	Executing from RAM or external memory			66	MHz
		Executing from Flash			50	
		Executing from Flash with RWW			45	
		Burst Mode disabled (FLASHLP bit =1)			33	
f_{PCLK}	Peripheral Clock for APB				33	
f_{CK}	Clock input pin				16	

2.7 nRSTIN Input Filter Characteristics

V_{33} = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 15. nRSTIN input Filter Characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
t_{FR}	nRSTIN Input Filtered Pulse				500	ns
t_{NFR}	nRSTIN Input Not Filtered Pulse		1.2			µs

2.8 Oscillator Electrical Characteristics

V_{33} = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Figure 9. Crystal Oscillator and Resonator

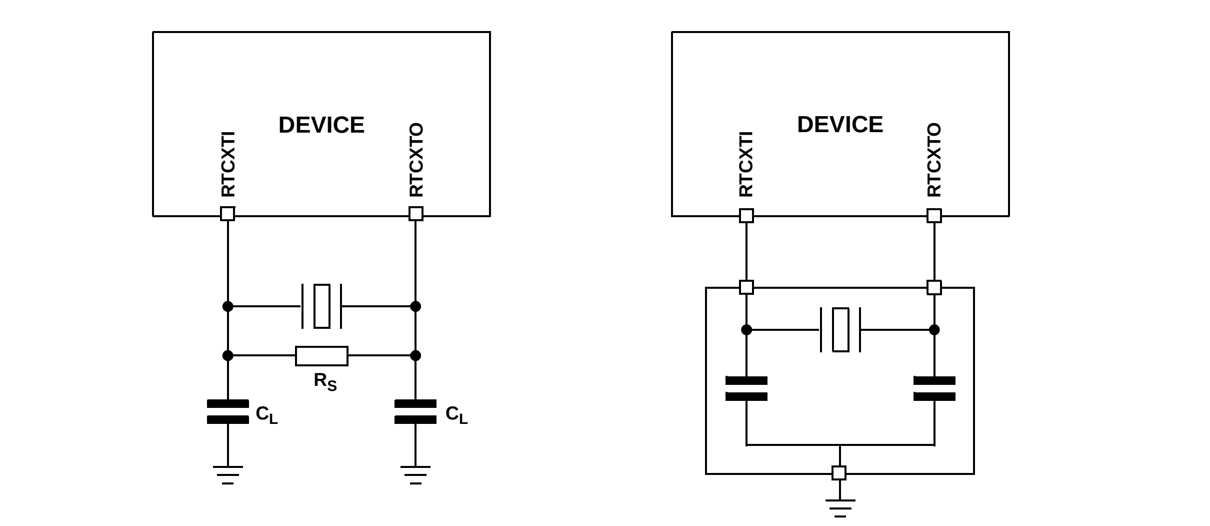


Table 16. Oscillator Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
g_m	Oscillator Transconductance			8		µA/V
t_{STUP}	Oscillator Start-up Time	Stable V_{33}			2.5	s

2.9 PLL Electrical Characteristics

V_{33} = 3.0 to 3.6V, $V_{33IOPLL}$ = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 17. PLL1 Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK1}$	PLL multiplier output clock	f_{PLL1}x 24			165	MHz
f_{PLL1}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1 MX[1:0]='00' or '01'	3.0		8.25	MHz
		FREF_RANGE = 1 MX[1:0]='10' or '11'	3.0		6	MHz
	PLL input clock duty cycle		25		75	%

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
f_{FREE1}	PLL free running frequency	FREF_RANGE = 0 MX[1:0]='01' or '11'		125		kHz
		FREF_RANGE = 0 MX[1:0]='00' or '10'		250		kHz
		FREF_RANGE = 1 MX[1:0]='01' or '11'		250		kHz
		FREF_RANGE = 1 MX[1:0]='00' or '10'		500		kHz
t_{LOCK1}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs
$\Delta t_{JITTER1}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

Table 18. PLL2 Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK2}$	PLL multiplier output clock	f_{PLL} x 28			140	MHz
f_{PLL2}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1	3.0		5	MHz
t_{LOCK2}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs
$\Delta t_{JITTER2}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

2.10 Flash Electrical characteristics

V_{33} = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 19. Flash Program/Erase Characteristics 1

Symbol	Parameter	Test Conditions	Value			Unit
			Typ	Max(C_0)	Max(C_{max})	
t_{PW}	Word Program		40			µs
t_{PDW}	Double Word Program		60			µs
t_{PB0}	Bank 0 Program (256K)	Double Word Program	1.6	2.1	4.3	s
t_{PB1}	Bank 1 Program (16K)	Double Word Program	130	170	300	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed Preprogrammed	2.3 1.9	4.0 3.3	4.9 4.1	s
t_{ES}	Sector Erase (8K)	Not preprogrammed Preprogrammed	0.7 0.6	1.1 1.0	1.36 1.26	s
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed Preprogrammed	8.0 6.6	13.7 11.2	17.2 14.0	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed Preprogrammed	0.9 0.8	1.5 1.3	1.87 1.66	s
t_{RPD}	Recovery from Power-Down				20	µs
t_{PSL}	Program Suspend Latency				10	µs
t_{ESL}	Erase Suspend Latency				300	µs

Note C_0: T_A = 85 °C *after 0 cycles*
C_{max}: T_A = 85 °C *after max number of cycles*

Table 20. Flash Program/Erase Characteristics 2

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
	Endurance (Bank 0 sectors)		10			kcycles
	Endurance (Bank1 sectors)		100			kcycles
	Data Retention		20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

2.11 External Memory Bus Timing

V_{33} = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

The tables below use a variable which is derived from the EMI_BCONn registers (described in the STR71x Reference Manual) and represents the special characteristics of the programmed memory cycle.

Symbol	Parameter	Value
t_{MCLK}	CPU clock period	1 / f_{MCLK}
t_C	Memory cycle time wait states	t_{MCLK} x (1 + [C_LENGTH])

Note: When f_{MCLK} is greater than or equal to 48 MHz, the EMI needs at least 1 wait state to work properly.

Table 21. EMI Read Operation

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
t_{RCR}	Read to CSn Removal Time			t_{MCLK}		ns
t_{RP}	Read Pulse Time			t_C		ns
t_{RDS}	Read Data Setup Time			t_C		ns
t_{RDH}	Read Data Hold Time			2		ns
t_{RAS}	Read Address Setup Time			1.5*t_{MCLK}		ns
t_{RAH}	Read Address Hold Time		0.65		2	ns
t_{RAT}	Read Address Turnaround Time			3		ns
t_{RRT}	RDn Turnaround Time			t_{MCLK}		ns

See Figure 10, Figure 11, Figure 12 and Figure 13 for related timing diagrams.

Table 22. EMI Write Operation

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
t_{WCR}	WEn to CSn Removal Time			t_{MCLK}		ns
t_{WP}	Write Pulse Time			t_C		ns
t_{WDS}	Write Data Setup Time			t_C + t_{MCLK}		ns
t_{WDH}	Write Data Hold Time			t_{MCLK}		ns
t_{WAS}	Write Address Setup Time			1.5*t_{MCLK}		ns
t_{WAH}	Write Address Hold Time			3		ns
t_{WAT}	Write Address Turnaround Time			3		ns
t_{WWT}	WEn Turnaround Time			t_{MCLK}		ns

See Figure 14, Figure 15, Figure 16 and Figure 17 for related timing diagrams.

Figure 10. Read Cycle Timing: 16-bit READ on 16-bit Memory

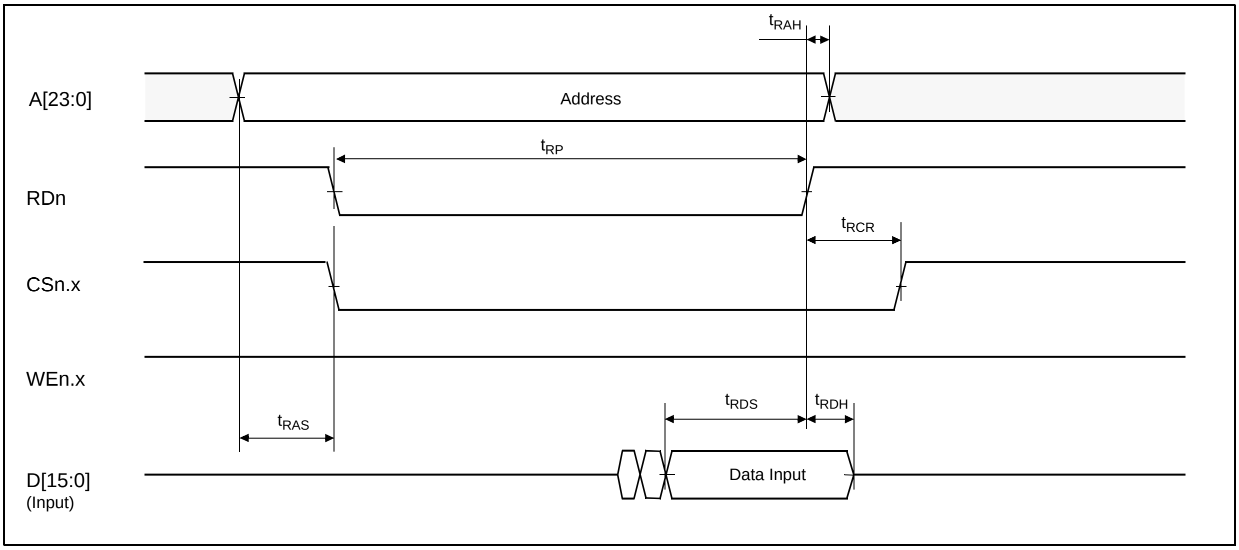
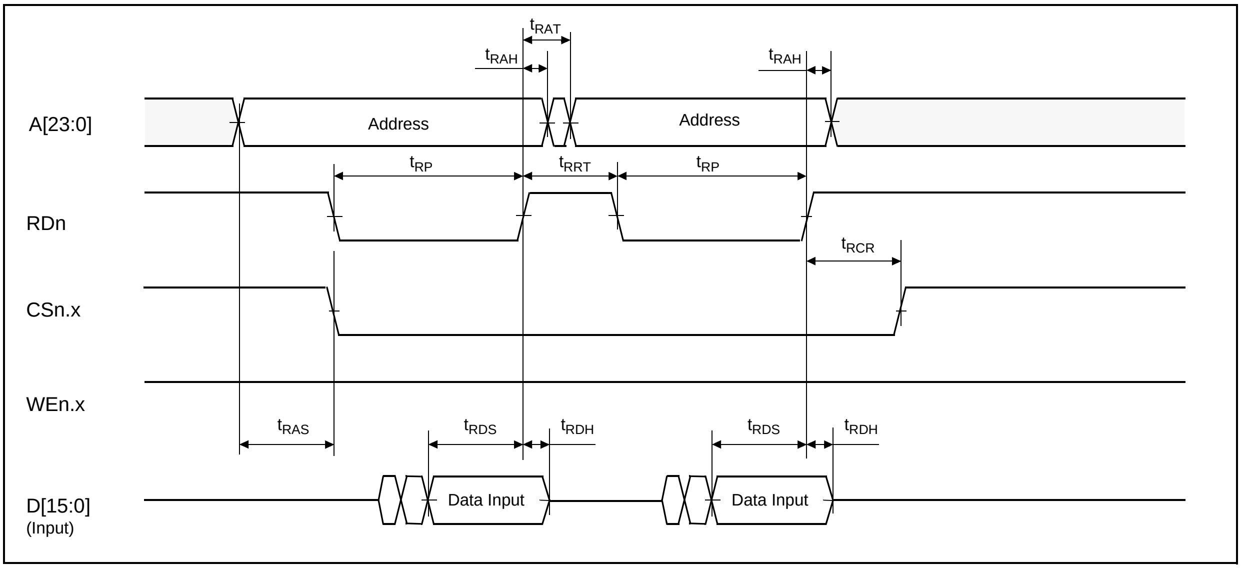


Figure 11. Read Cycle Timing: 32-bit READ on 16-bit Memory



See Table 21 for read timing data.

Figure 12. Read Cycle Timing: 16-bit READ on 8-bit Memory

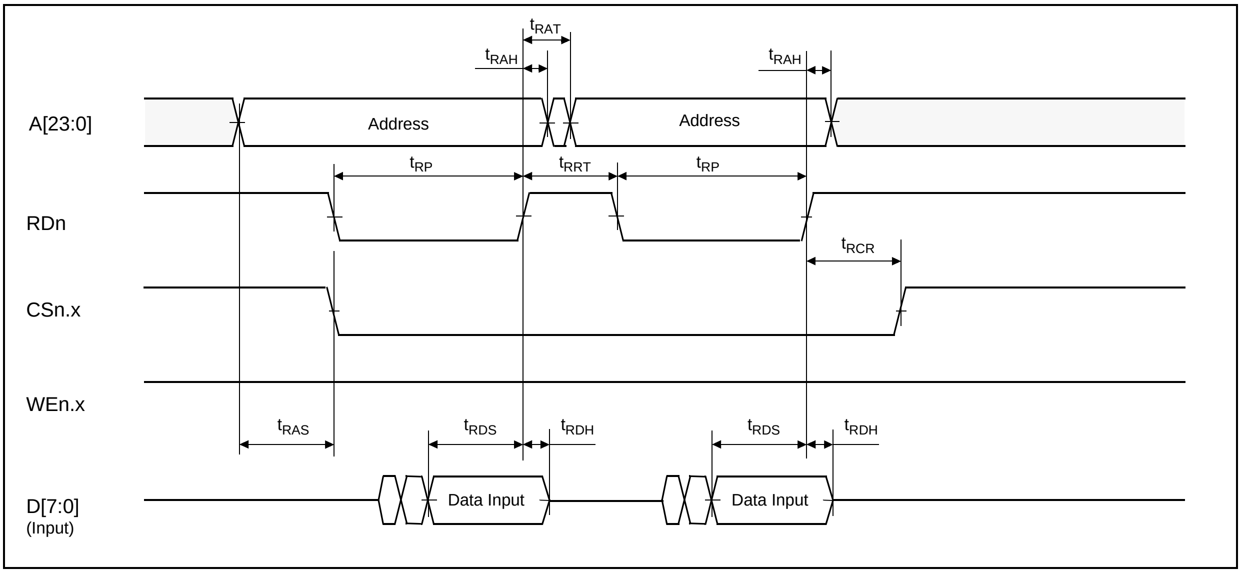
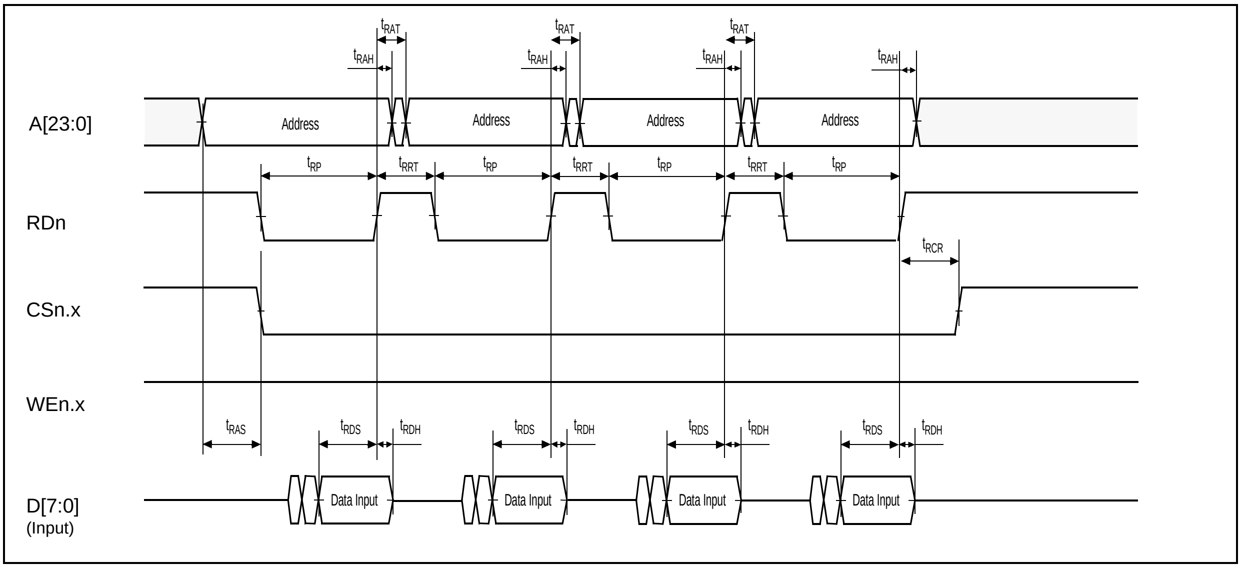


Figure 13. Read Cycle Timing: 32-bit READ on 8-bit Memory



See Table 21 for read timing data.

Figure 14. Write Cycle Timing: 16-bit WRITE on 16-bit Memory

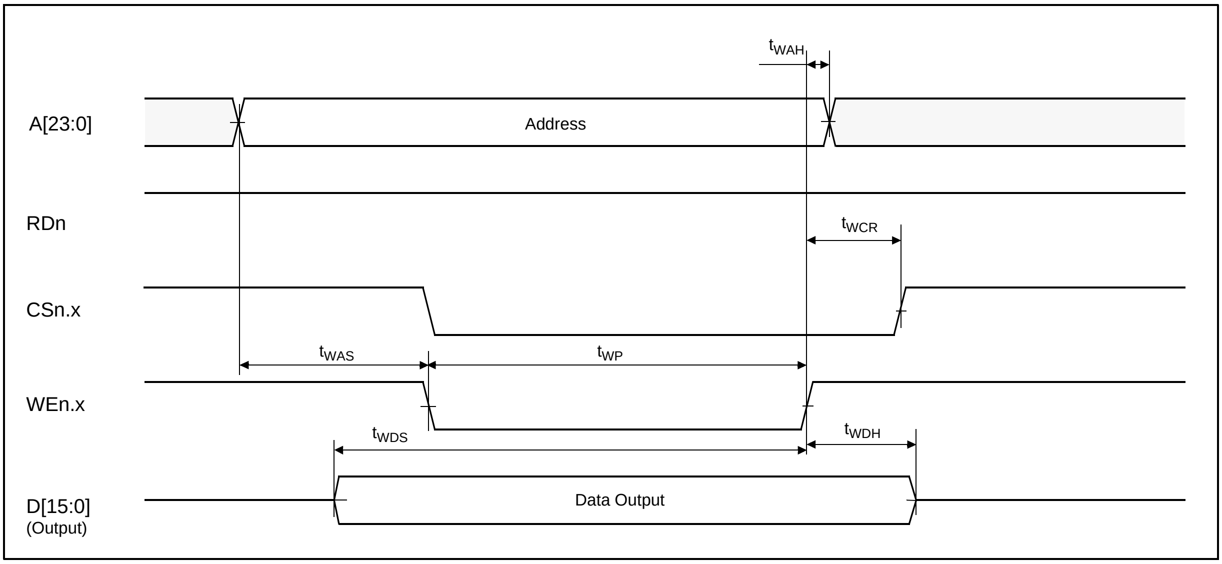
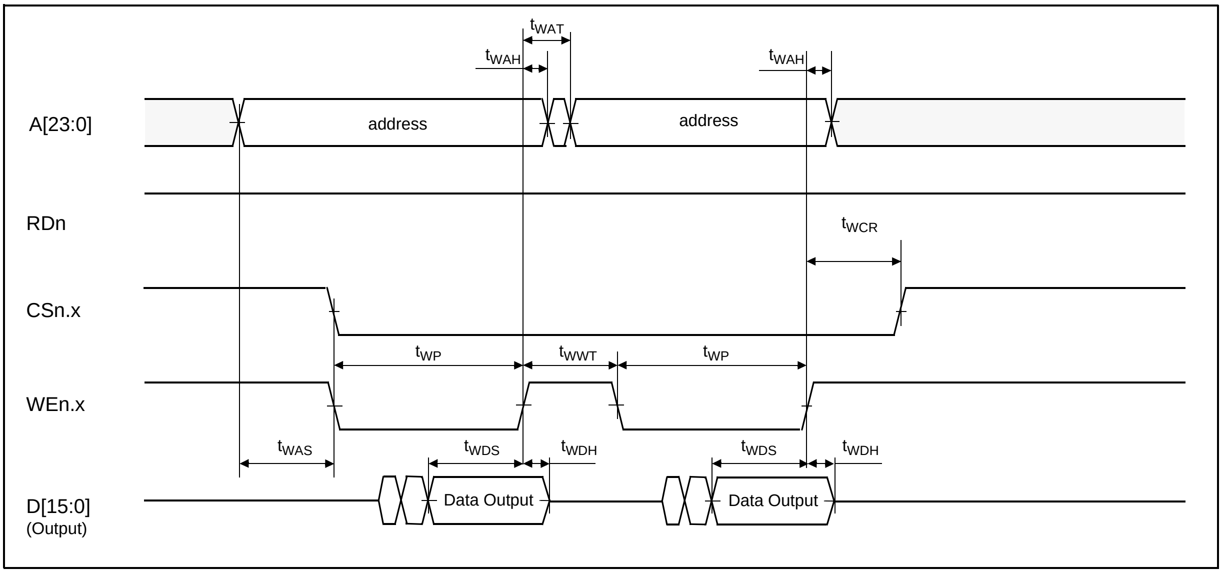


Figure 15. Write Cycle Timing: 32-bit WRITE on 16-bit Memory



See Table 22 for write timing data.

Figure 16. Write Cycle Timing: 16-bit WRITE on 8-bit Memory

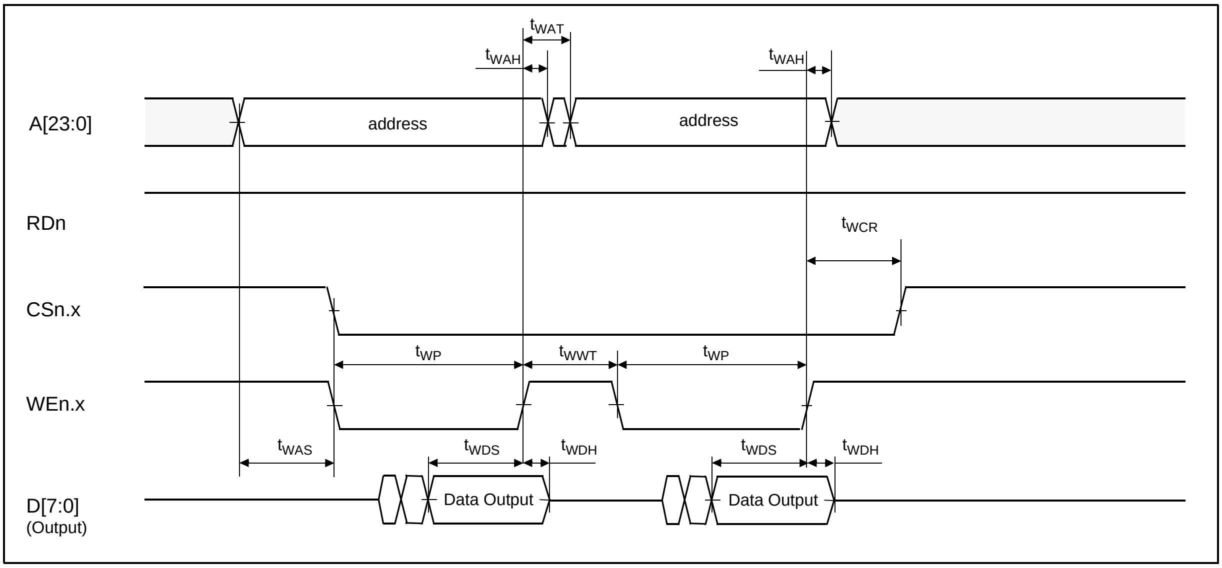
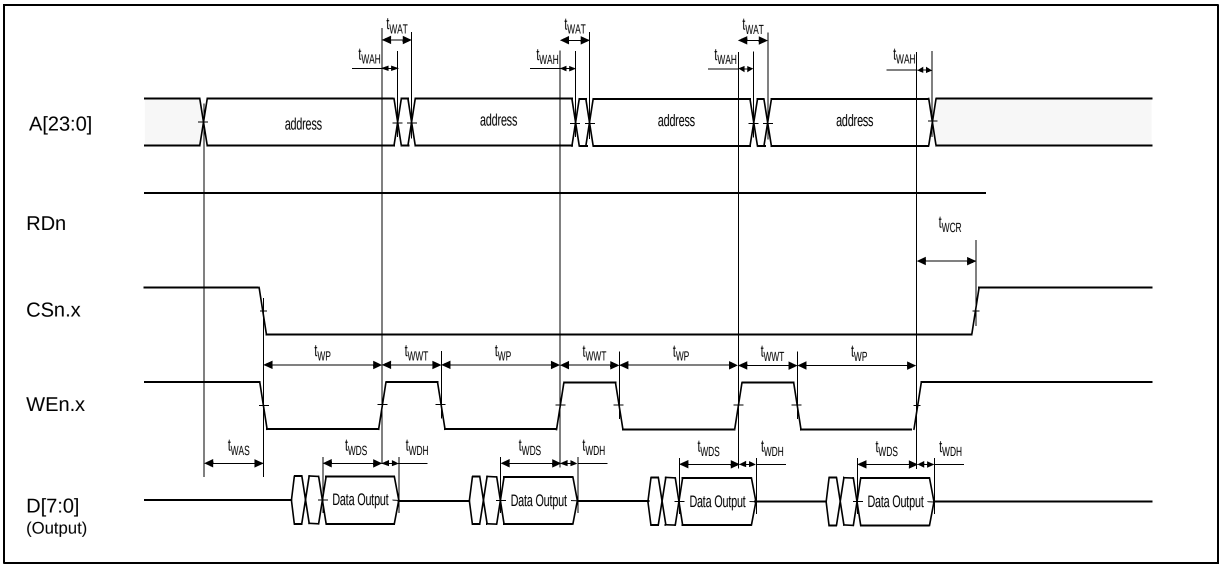


Figure 17. Write Cycle Timing: 32-bit WRITE on 8-bit Memory



See Table 22 for write timing data.

2.12 USB Characteristics

The USB interface is USB-IF certified.

2.13 ADC Electrical Characteristics

V_{33} = 3.0 to 3.6V, AV_{DD} = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

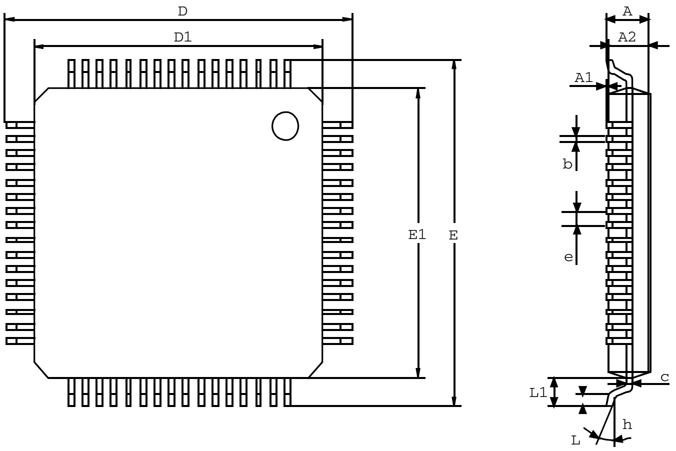
Table 23. ADC Electrical Characteristics

Symbol	Parameter	Test Conditions	Value Min	Value Typ	Value Max	Unit
RES	Resolution	Sinewave with ΔV_{IN} amplitude		12		bits
ΔV_{IN}	Input Voltage Range		0		2.5	V
f_{MOD}	Modulator Oversampling Frequency				2.1	MHz
t_{CONV}	Conversion time		4096/ f_{MOD}(max)			µs
N_{ch}	Number of Input Channels				4	n
PBR	Passband Ripple				0.1	dB
SINAD	S/N and Distortion		56	63		dB
THD	Total Harmonic Distortion		60	74		dB
Z_{IN}	Input Impedance	f_{MOD}				

3 PACKAGE CHARACTERISTICS

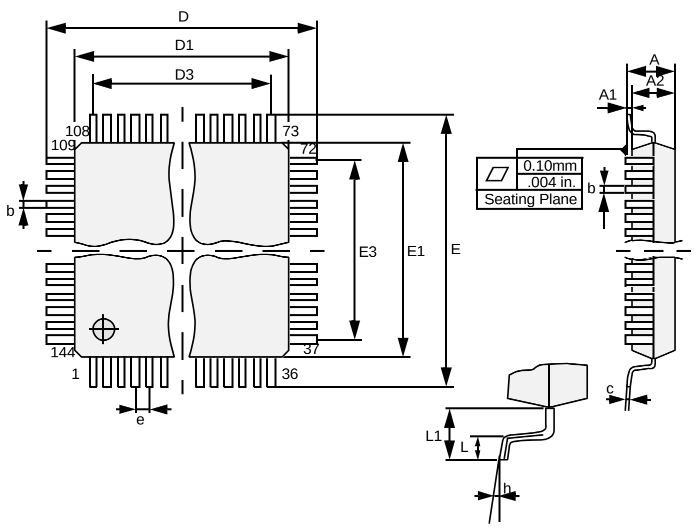
3.1 Package Mechanical Data

Figure 18. 64-Pin Thin Quad Flat Package (10x10)



Dim.	mm			inches		
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	64					

Figure 19. 144-Pin Thin Quad Flat Package

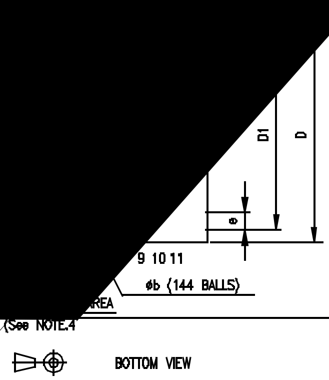


Dim.	mm			inches		
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053		0.057
b	0.17	0.22	0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	21.80	22.00	22.20	0.858	0.867	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D3		17.50			0.699	
E	21.80	22.00	22.20	0.858	0.867	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E3		17.50			0.699	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	144					

Figure 2[redacted]

[redacted]

Figure [redacted]



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	1.21		1.70	0.048		0.067
A1	0.21			0.008		
A2		1.12			0.044	
b	0.35	0.40	0.45	0.014	0.016	0.018
D	9.85	10.00	10.15	0.388	0.394	0.400
D1		8.80			0.346	
E	9.85	10.00	10.15	0.388	0.394	0.400
E1		8.80			0.346	
e		0.80			0.031	
F		0.60			0.024	
ddd			0.10			0.004
eee			0.15			0.006
fff			0.08			0.003
	Number of Pins					
N	144					

3.2 Thermal Characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$T_J = T_A + (P_D \times \Theta_{JA})$ (1)

Where:

– T_A is the Ambient Temperature in °C,
– Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
– P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
– P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.
– $P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$P_D = K / (T_J + 273°C)$ (2)

Therefore (solving equations 1 and 2):

$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2$ (3)

where:

– K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 24. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** TQFP 144 - 20 x 20 mm / 0.5 mm pitch	42	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** TQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 144 - 10 x 10 x 1.7mm	50	°C/W

4 ORDER CODES

Table 25. Order Codes

<table>
<tr><th>Partnumber</th><th>FLASH Kbytes</th><th>RAM Kbytes</th><th>EMI</th><th>USB</th><th>CAN</th><th>I/O Ports</th><th>Package</th><th>Temp. Range</th></tr>
<tr><td>STR710FZ1T6</td><td>128+16</td><td>32</td><td rowspan="2">Yes</td><td rowspan="2">Yes</td><td rowspan="2">Yes</td><td rowspan="2">48</td><td rowspan="2">TQFP144 20 x 20</td><td rowspan="18">-40 to +85°C</td></tr>
<tr><td>STR710FZ2T6</td><td>256+16</td><td>64</td></tr>
<tr><td>STR710FZ1H6</td><td>128+16</td><td>32</td><td rowspan="2">Yes</td><td rowspan="2">Yes</td><td rowspan="2">Yes</td><td rowspan="2">48</td><td rowspan="2">LFBGA 10 x 10 1.7</td></tr>
<tr><td>STR710FZ2H6</td><td>256+16</td><td>64</td></tr>
<tr><td>STR711FR0H6</td><td>64+16</td><td>16</td><td rowspan="14">No</td><td rowspan="6">Yes</td><td rowspan="6">No</td><td rowspan="6">30</td><td rowspan="3">LFBGA64 8 x 8 1.7</td></tr>
<tr><td>STR711FR1H6</td><td>128+16</td><td>32</td></tr>
<tr><td>STR711FR2H6</td><td>256+16</td><td>64</td></tr>
<tr><td>STR711FR0T6</td><td>64+16</td><td>16</td><td rowspan="3">TQFP64 10x10</td></tr>
<tr><td>STR711FR1T6</td><td>128+16</td><td>32</td></tr>
<tr><td>STR711FR2T6</td><td>256+16</td><td>64</td></tr>
<tr><td>STR712FR0H6</td><td>64+16</td><td>16</td><td rowspan="8">No</td><td rowspan="6">Yes</td><td rowspan="8">32</td><td rowspan="3">LFBGA64 8 x 8 1.7</td></tr>
<tr><td>STR712FR1H6</td><td>128+16</td><td>32</td></tr>
<tr><td>STR712FR2H6</td><td>256+16</td><td>64</td></tr>
<tr><td>STR712FR0T6</td><td>64+16</td><td>16</td><td rowspan="3">TQFP64 10 x10</td></tr>
<tr><td>STR712FR1T6</td><td>128+16</td><td>32</td></tr>
<tr><td>STR712FR2T6</td><td>256+16</td><td>64</td></tr>
<tr><td>STR715FR0H6</td><td>64+16</td><td>16</td><td rowspan="2">No</td><td>LFBGA64 8 x 8 1.7</td></tr>
<tr><td>STR715FR0T6</td><td>64+16</td><td>16</td><td>TQFP64 10 x 10</td></tr>
</table>

5 REVISION HISTORY

Table 26. Revision history

Date	Revision	Description of Changes
17-Mar-2004	1	First Release
05-Apr-2004	2	Updated “ELECTRICAL CHARACTERISTICS” on page 30
08-Apr-2004	2.1	Corrected STR712F Pinout. Pins 43/42 swapped.
15-Apr-2004	2.2	PDF hyperlinks corrected.
7-Jul-2004	3	Corrected description of STDBY, V18, VSS18 V18BKP VSSBKP pins Added IDDrun typical data Updated BSPI max. baudrate. Updated “External Memory Bus Timing” on page 39
29-Oct-2004	4	Corrected Flash sector B1F0/F1 address in Figure 6 on page 27 Corrected Table 6 on page 22 TQFP64 TEST pin is 16 instead of 17. Added to TQPFP64 column: pin 7 BOOTEN, pin 17 $V_{33IO\text{-}PLL}$ Changed description of JTCK from ‘External pull-down required’ to ‘External pull-up or pull down required’.
25-Jan-2005	5	Changed “Product Preview” to “Preliminary Data” on page 1 and 3 Renamed ‘PU/PD’ column to ‘Reset state’ in Table 6 on page 22 Added reference to STR7 Flash Programming Reference Manual
19-Apr-2005	6	Added STR715F devices and modified RAM size of STR71xF1 devices Added BGA package in Section 3 Updated ordering information in Section 4 . Added PLL duty cycle min and max. in Section 2.9
13-Oct-2005	7	Updated feature description on page 1 Update overview Section 1.1 Added OD/PP to P0.12 in Table 6 Changed name of WFI mode to WAIT mode Changed Memory Map Table 6: Ext. Memory changed to 64 MB and flash register changed to 36 bytes. Added Power Consumption Table 13 Modified BGA144 F3, F5, F12 and G12 in Table 2 and Table 3 Update EMI Timiing Table 21, Table 22 and Figure 14

Notes:

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